JW5079A

23V/10A

Sync. Step-Down Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®5079A is a monolithic buck switching regulator based on I2 architecture for fast transient response. Operating with an input range of 4V~23V, JW5079A delivers 10A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. At light loads, the regulator operates in low frequency to maintain high efficiency and low output ripples.

JW5079A guarantees robustness with output short protection, thermal protection, current run-away protection, and input under voltage lockout.

JW5079A is available in QFN3×3-20 package, which provide a compact solution with minimal external components.

FEATURES

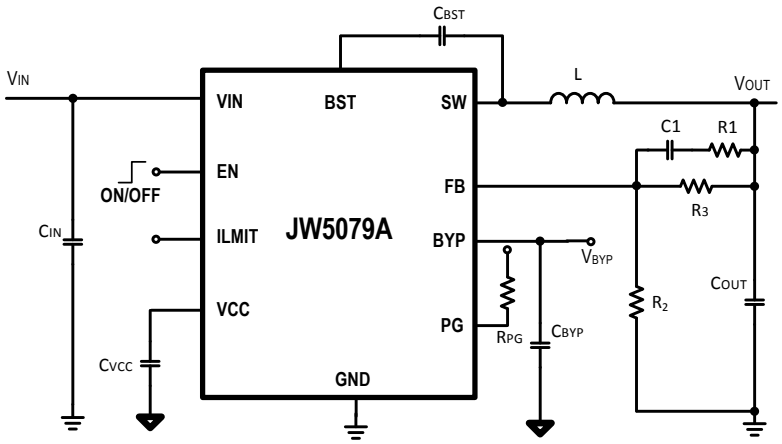
- 4V to 23V operating input range
  10A continuous
- Up to 95% efficiency
- High efficiency at light load
- 500kHz switching frequency
- External bypass input
- Programmable valley current limit
- Power good indicator
- Input under voltage lockout
- Output discharge function
- Output over voltage latch off protection
- Output short protection
- Thermal protection
- Available in QFN3X3-20 package

APPLICATIONS

- Industrial and commercial low power system
- Notebook
- LDO monitors and TVs
- Green electronics/appliances

TYPICAL APPLICATION

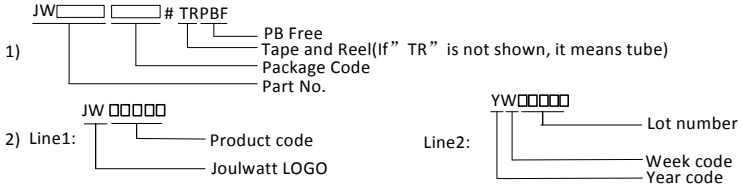
10A Step-down Regulator



ORDER INFORMATION

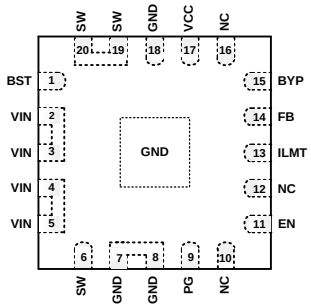
DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW5079AQFNF#TRPBF	QFN3X3-20	JW5079A YW□□□□□

Notes:



PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

VIN, EN, PG, SW, ILMT Pin..... -0.3V to 28V
BST Pin ..... SW-0.3V to SW+5V
All other Pins ..... -0.3V to 6V
Junction Temp. [2)] 150ºC
Lead Temperature 260ºC
ESD Susceptibility (Human Body Model) 2kV

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage VIN ..... 4V to 23V
Output Voltage V_{OUT}.....0.6V to VIN-3V
Ambient Temperature Range ..... -40°C to 85°C

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
QFN3X3-20	30	4.5ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JW5079A includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VIN=12V, T_A=25℃, Unless otherwise stated.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IN} Under Voltage Lock-out Threshold	V_{IN_MIN}	V_{IN} rising	2.7	2.91	3.12	V
		V_{IN} falling	2.45	2.7	2.95	V
V_{IN} Under voltage Lockout Hysteresis	$V_{IN\_MIN\_HYST}$			180		mV
Shutdown Current	I_{SD}	V_{EN}=0V		2	5	μA
Supply Current	I_Q	V_{EN}=5V, V_{BYP}=5V		45	70	μA
EN Rising Threshold	V_{EN_H}		0.8			V
EN Falling Threshold	V_{EN_L}				0.4	V
Feedback Voltage	V_{FB}	4V<V_{VIN}<23V	594	600	606	mV
Top Switch Resistance[5]	$R_{DS(ON)T}$			18		mΩ
Bottom Switch Resistance[5]	$R_{DS(ON)B}$			8		mΩ
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=23V, V_{SW}=0V			1	μA
Bottom Switch Leakage Current	I_{LEAK_BOT}	V_{IN}=23V, V_{SW}=23V			2	μA
Bottom Switch Current Limit	I_{LIM}	I_{LIM} ="0"	10			A
		I_{LIM} =Floating	13			A
		I_{LIM} ="1"	17			A
ILMIT Rising Threshold[5]	V_{LIMTH}		VCC-0.8		VCC	V
ILMIT Falling Threshold[5]	V_{LIMTL}				0.8	V
Minimum On Time[5]	T_{ON_MIN}			100		ns
Minimum Off Time	T_{OFF_MIN}	V_{FB}=0.4V		100		ns
Switching Frequency [5]	Fs			500		kHz
Discharge FET Ron	R_{DIS}			50		Ω
Soft-Start Time[5]	T_{SS}			400		us
VCC Output	V_{CC}	V_{IN}=12V	4.7	5	5.25	V
Power Good Threshold	$PGD_{\_TH}$	V_{FB} Rising	92.5%	95%	98.5%	V_{REF}
Power Good Hysteresis[5]	$PGD_{\_HYS}$			5%		V_{REF}
Power Good Delay Time[5]	$PGD_{\_DLY}$	Low to high		300		us
		High to low		10		us
Power Good Sink Current	I_{PG}	PG=0.5V	2			mA
Output Over-voltage Threshold		V_{FB} Rising	115%	120%	125%	V_{REF}
Output Over-voltage Hysteresis[5]				5%		V_{REF}
Output Over-voltage Delay Time[5]				20		us
Output Under-voltage Threshold		V_{FB} Falling	55%	60%	65%	V_{REF}
Output Under-voltage Delay Time[5]		FB forced below UV threshold		100		us

VIN=12V, T_A=25℃，Unless otherwise stated.						
Item	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Bypass Switch Ron	R_{BYP}			9.5		Ω
Bypass Switch Turn-on Voltage	V_{BYP_ON}		4.47	4.7		V
Bypass Switch Switchover Hysteresis[5)]	V_{BYP_HYS}			0.2		V
Thermal Shutdown[5)]	T_{TSD}			150		°C
Thermal Shutdown hysteresis[5)]	T_{TSD_HYST}			15		°C

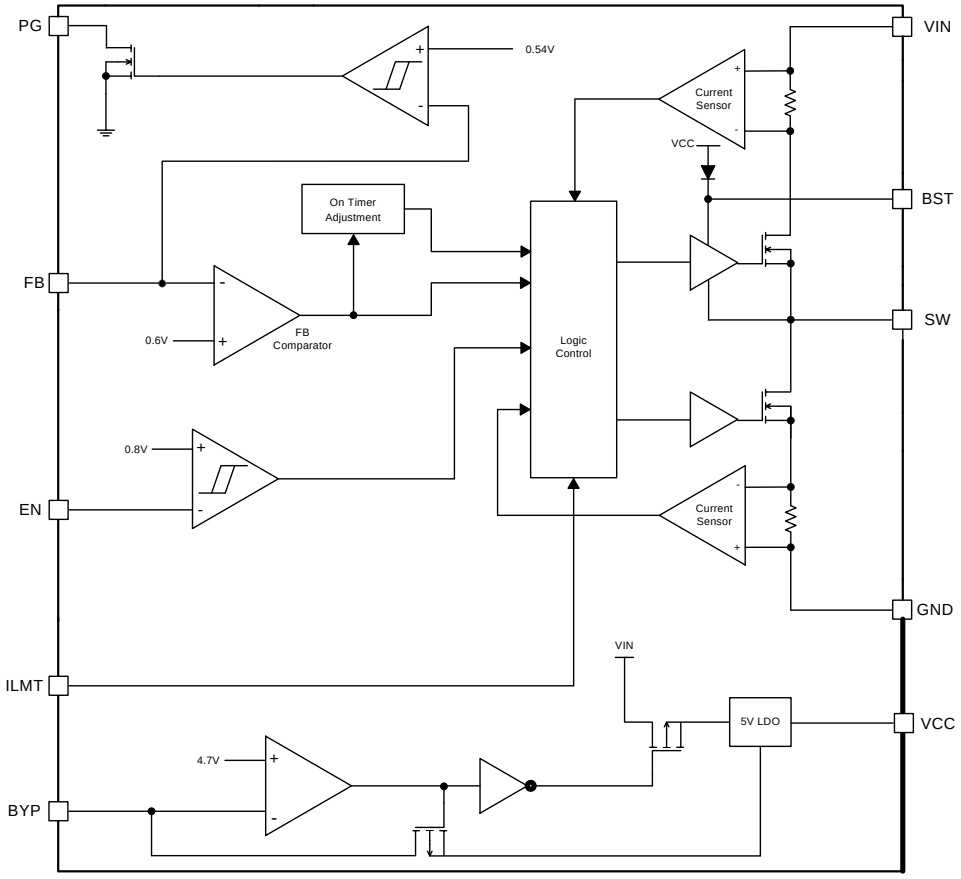
Note：

5) Guaranteed by design.

PIN DESCRIPTION

Pin	Name	Description
1	BST	Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.
2,3,4,5	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4V to 23V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
6,19,20	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
7,8,18,EP	GND	Ground pin
9	PG	Power good monitor output. This is an open-drain output so a resistor should be connected at this pin to the VCC pin.
11	EN	Enable Control. Pull this pin high to turn on the Buck. Do not leave this pin floating.
10,12,16	NC	
13	ILMT	Current Limit Setting Pin. The current limit is set to 10A, 13A or 17A when this pin is pull low, floating or pull high respectively.
14	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.6V. Connect a resistive divider at FB.
15	BYP	Bypass input for the internal LDO. BYP is externally connected to the output of switching regulator. When the BYP voltage rises above the bypass switch turn-on threshold, the power supply of the internal LDO regulator changes to the external source.
17	VCC	5V Linear Regulator Output for Internal Control Circuit. A capacitor (typical 2.2uF) should be connected to GND. Don’t connect to external Load.

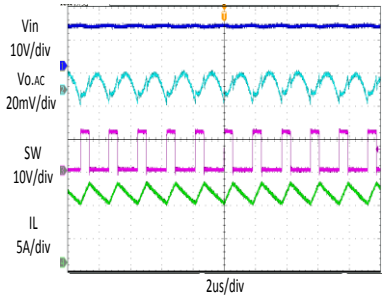
BLOCK DIAGRAM



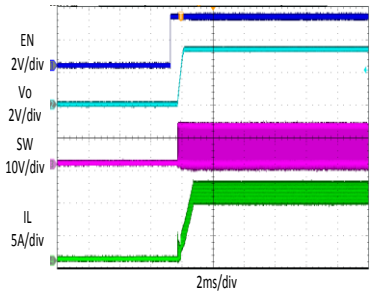
TYPICAL PERFORMANCE CHARACTERISTICS

VIN =12V, VOUT= 3.3V, L = 1.5μH, Cout = 4*22μF,TA = +25°C, unless otherwise noted

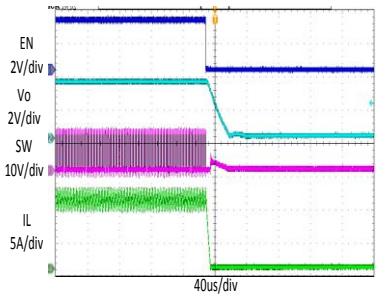
Steady State Test
VIN=12V, VOUT=3.3V
IOUT =8A



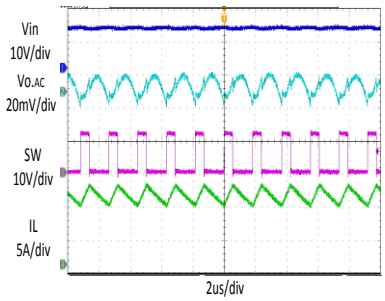
Startup through Enable
VIN=12V, VOUT =3.3V
IOUT =8A



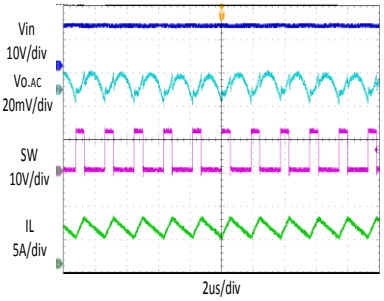
Shutdown through Enable
VIN=12V, VOUT =3.3V
IOUT =8A



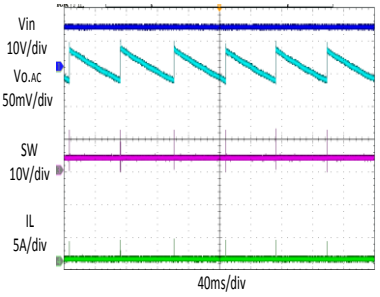
Heavy Load Operation
8A LOAD



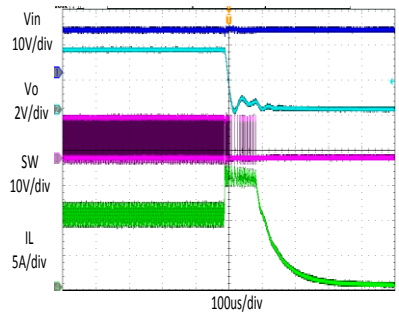
Medium Load Operation
4A LOAD



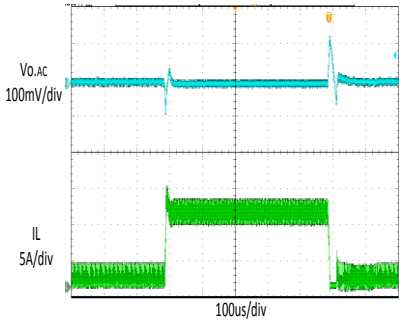
Light Load Operation
0 A LOAD



Short Circuit Protection
VIN=12V, VOUT =3.3V
IOUT =8A- Short



Load Transient
C1=10pF,R1=0k
0.8A LOAD → 8A LOAD → 0.8A LOAD



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

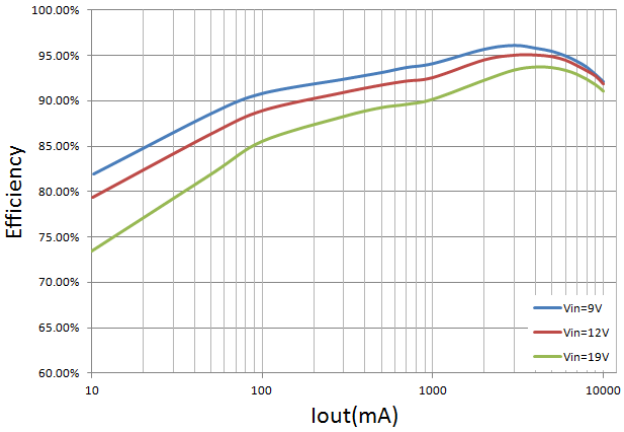


Figure 1. Efficiency vs Load Current

(Vout=3.3V, L=1.5uH)

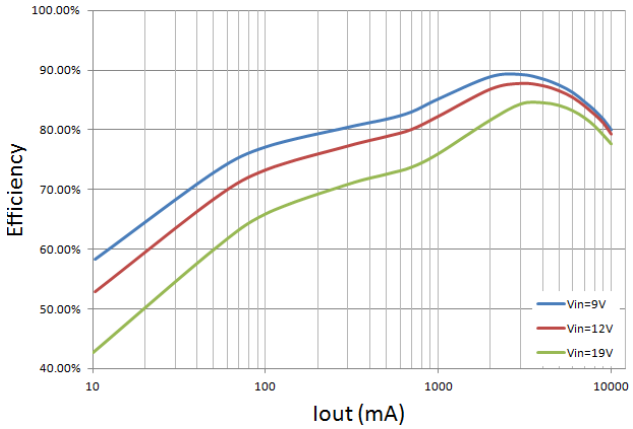


Figure 2. Efficiency vs Load Current

(Vout=1V, L=1uH)

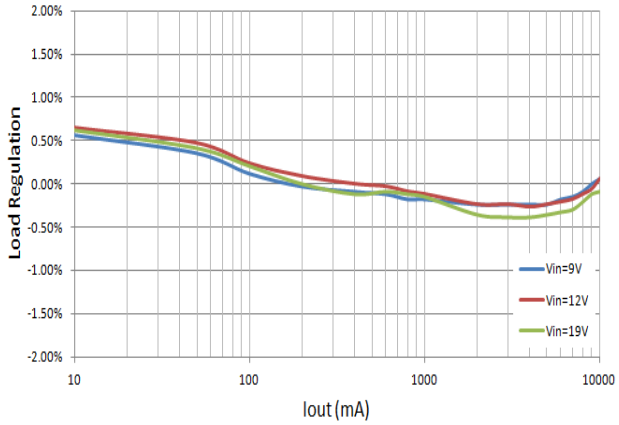


Figure 3. Load regulation vs Load Current

(Vout=3.3V, L=1.5uH)

FUNCTIONAL DESCRIPTION

JW5079A is a synchronous step-down regulator based on I2 control architecture. It regulates input voltages from 4V to 23V down to an output voltage as low as 0.6V, and is capable of supplying up to 10A continuous load current.

Power Switch

N-Channel MOSFET switches are integrated on the JW5079A to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage greater than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the VCC when SW is low.

Vin Under-Voltage Protection

In addition to the enable function, the JW5079A provides an Under Voltage Lock-out (UVLO) function that monitors the input voltage. To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when input voltage drops below the UVLO-falling threshold. The IC resumes switching when input voltage exceeds the UVLO-rising threshold.

Soft Start

The JW5079A has an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start, it clamps the ramping of internal reference voltage which is compared with FB signal. The typical soft-start duration is 0.4ms.

Enable and Disable

The JW5079A's EN is used to control converter, the enable voltage (EN) has low and high threshold voltage. When VEN is below its high threshold voltage, the IC enters shutdown mode. When VEN exceeds its high threshold voltage, the converter is fully operational. In shutdown mode, the entire regulator of JW5079A is off.

Power Good

The JW5079A has power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect to Vcc or another voltage source through a resistor. It is high if the output voltage is higher than 95% and lower than 120% of the nominal voltage.

Output Voltage Over-voltage Protection

JW5079A integrates both output over-voltage protection and under-voltage protection. If the output voltage rises above the regulation level, the high-side MOSFET naturally remains off and the synchronous rectifier will turn on until the inductor current reaches the zero. If the output voltage exceeds the OVP threshold for longer than 20 us (typical), the OVP function is triggered. If the output voltage drops below the UVP trip threshold for longer than 100 us (typical), the UVP function is triggered.
JW5079A use latch-off mode in OVP and UVP. When the protection function is triggered, the IC will shut down. The IC stops switching and is latched off. To restart operation, toggle EN or power the IC off and then on again.

Current Limit

The JW5079A current limit is adjustable (10A,13A,17A) by ILMT pin and it is a cycle-by-cycle " valley " mechanism, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. The current is determined by measuring the voltage between source and drain of the synchronous rectifier, adding temperature compensation for greater

accuracy. If the current exceeds the current limit, the turn-on signal of top MOSFET is inhibited until the inductor current ramps down below the current limit. Thus, only when the inductor current is well below the current limit, another on-time is permitted. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If it drops below the output under-voltage protection level, the IC will stop switching to avoid excessive heat.

Linear Regulator (VCC)

The JW5079A integrates a 5V linear regulator (VCC). When the input voltage of BYP pin is lower than the switch over threshold 4.7V, the VCC regulator steps down input voltage to supply both internal circuitry and gate drivers. When the input voltage of BYP pin is higher than the switch over threshold 4.7V, an automatic circuit will change the power source of linear regulator from VIN path to external path, therefore the power dissipation of linear regulator will be decrease efficiently. A 2.2uF ceramic capacitor is recommended to bypass VCC to GND. Do not connect the VCC pin to external loads.

Thermal Protection

When the temperature of the JW5079A rises above 150°C, it is forced into thermal protection (OTP). The JW5079A uses latch-off mode in OTP. When the protection function is triggered, the IC will shut down. The IC stops switching and is latched off. To restart operation, toggle EN or power the IC off and then on again.

APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} * \frac{R_2}{R_2 + R_3}$$

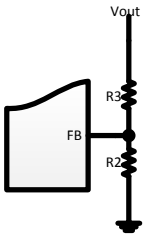
where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Choose R_2 around 15kΩ, and then R_3 can be calculated by:

$$R_3 = R_2 * \left(\frac{V_{OUT}}{0.6} - 1\right)$$

Too large resistance and the following table lists the recommended values.

V_{OUT}(V)	R2(kΩ)	R3(kΩ)
1	10	6.65
1.2	10	10
1.5	10	15
2.5	17.8	56.2
3.3	17.8	80.6
5	17.8	130



Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{CIN} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where I_{OUT} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{OUT}}{f_S * \Delta V_{IN}} * \frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_{IN} is the input capacitance value, f_S is the switching frequency, $\triangle V_{IN}$ is the input ripple voltage. The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 10uF*4 ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S * L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) * \left(R_{ESR} + \frac{1}{8 * f_S * C_{OUT}}\right)$$

where C_{OUT} is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage. The output capacitors also affect the system stability and transient response, and a 66uF~88uF ceramic capacitor is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the

ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S * \Delta I_L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

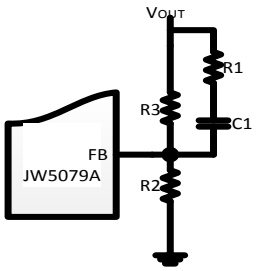
where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_S is the switching frequency, and $\triangle I_L$ is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

A bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1uF low ESR ceramic capacitor is recommended to connected to the BST pin and SW pin.

Feedforward Capacitor

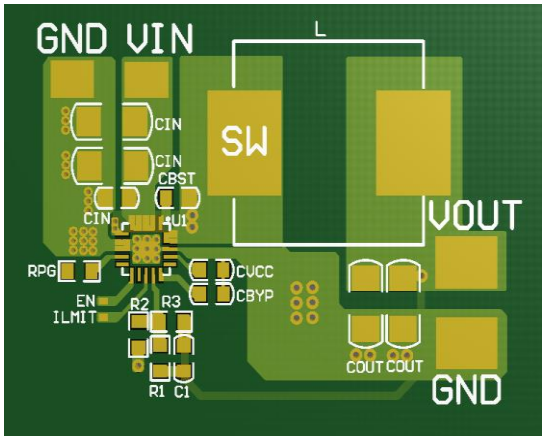
In order to minimize the ripple of output voltage at load transient, a feedforward capacitor in series with a resistor should be in parallel to the upper divider resistor. Choose R_1 around 0kΩ and C1 around 10pF.



PCB Layout Note

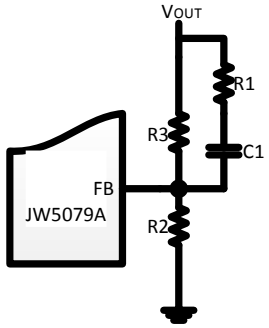
For minimum noise problem and best operating performance, We should place the following components close to the IC: C_{IN}, C_{VCC},L,R2 and R3.

1. Place the input decoupling capacitor as close to JW5079A (VIN pin and GND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as far away from the inductor and noisy power traces as possible.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.



External Components Suggestion:

V_{out}(V)	R2 (kΩ)	R3 (kΩ)	R1 (kΩ)	C1 (pF)	L(uH)	C_{OUT}(uF)
1	10	6.65	0	10	1	66~88
1.2	10	10	0	10	1	66~88
1.5	10	15	0	10	1	66~88
2.5	17.8	56.2	0	10	1.5	66~88
3.3	17.8	80.6	0	10	1.5	66~88
5	17.8	130	0	10	1.5	66~88



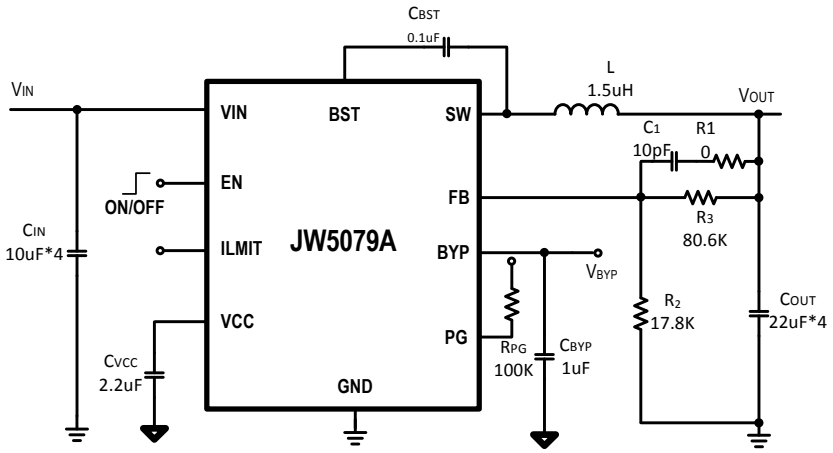
REFERENCE DESIGN

Reference 1:

VIN : 4V~23V

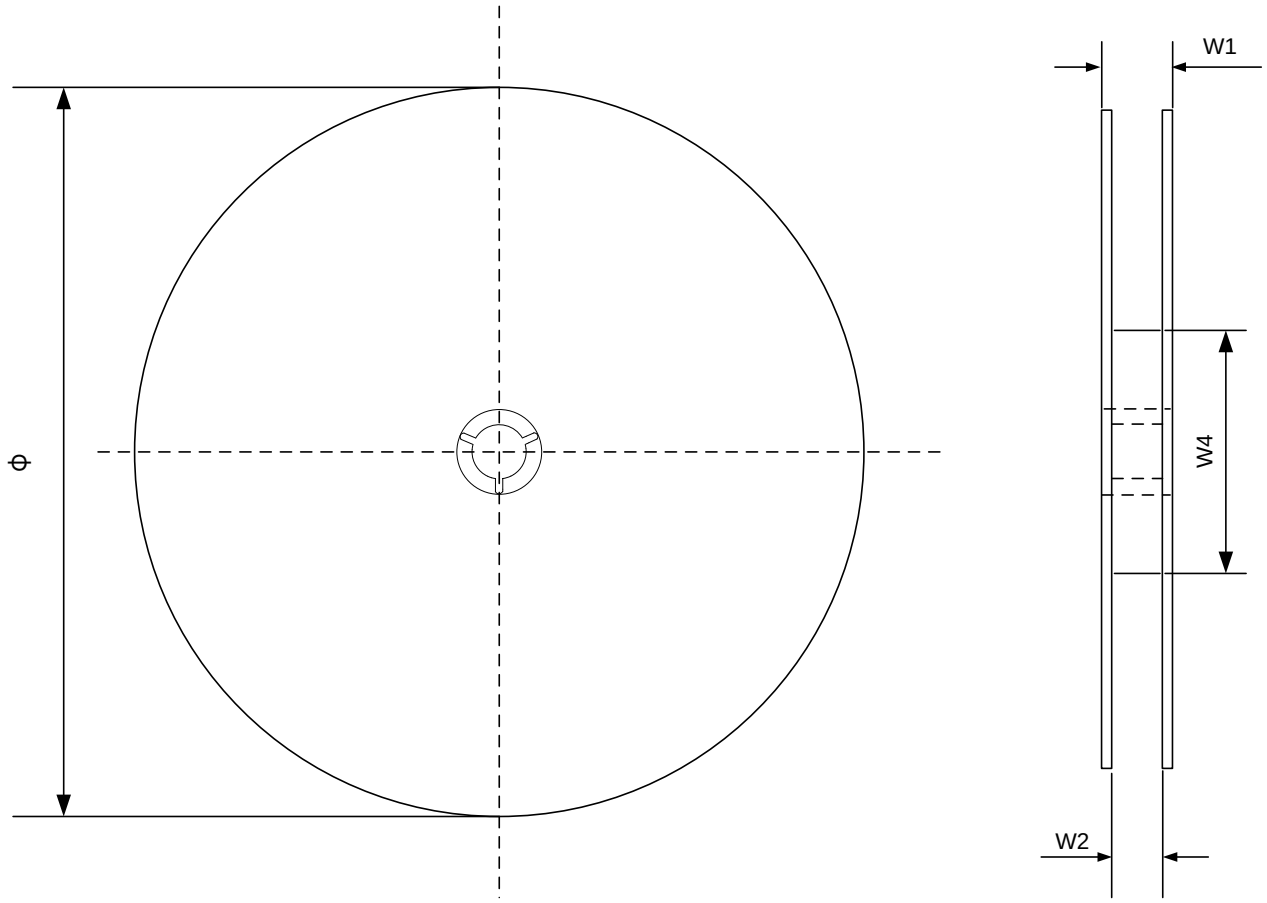
VOUT: 3.3V

IOUT: 0~10A



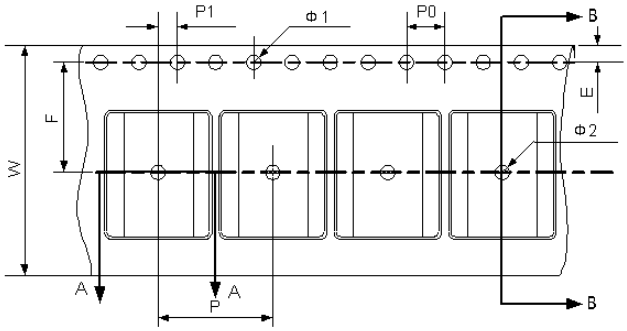
TAPE AND REEL INFORMATION

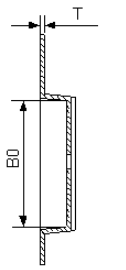
Reel UNIT: mm



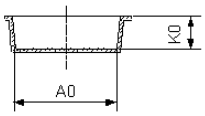
封装形式	直径 Φ	厚度 W1	宽度 W2	W4
QFN3×3-20	330±2	17.6±2	12.4±2	100±2

Carrier Tape UNIT: mm





SECTION B-B

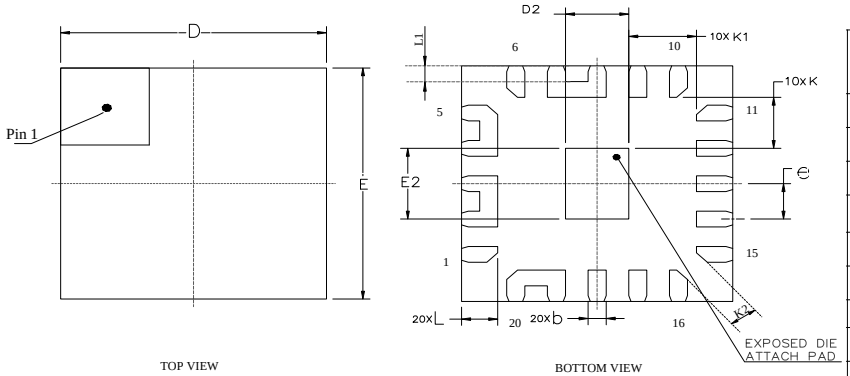


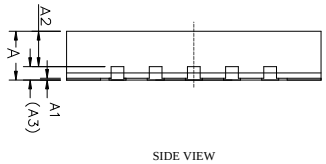
SECTION A-A

封装形式	P0	P1	P	A0	B	W	T0	K0	Φ1	Φ2	E	F
QFN3x3-20	4.0±0.1	2.0±0.1	8.0±0.2	3.30±0.2	3.30±0.2	12.0±0.3	0.25±0.20	0.75±0.2	1.50min	1.50min	1.75±0.1	5.50±0.10

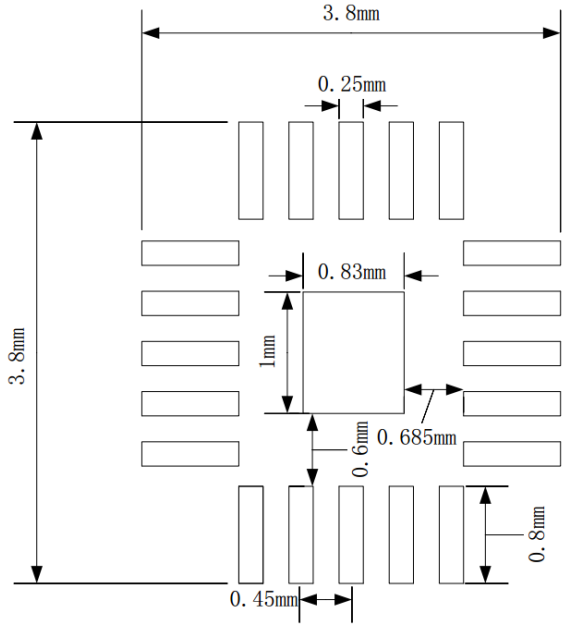
PACKAGE OUTLINE

QFN3X3-20 UNIT: mm





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
A2	---	0.40	---
A3		0.152 REF	
b	0.15	0.20	0.25
D		3.00 BSC	
E		3.00 BSC	
e		0.45 BSC	
D2	0.60	0.70	0.80
E2	0.80	0.90	1.00
L	0.30	0.40	0.50
L1		0.20 REF	
K		0.65 REF	
K1		0.75 REF	
K2		0.311 REF	



Recommended PCB layout
(Reference only)

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